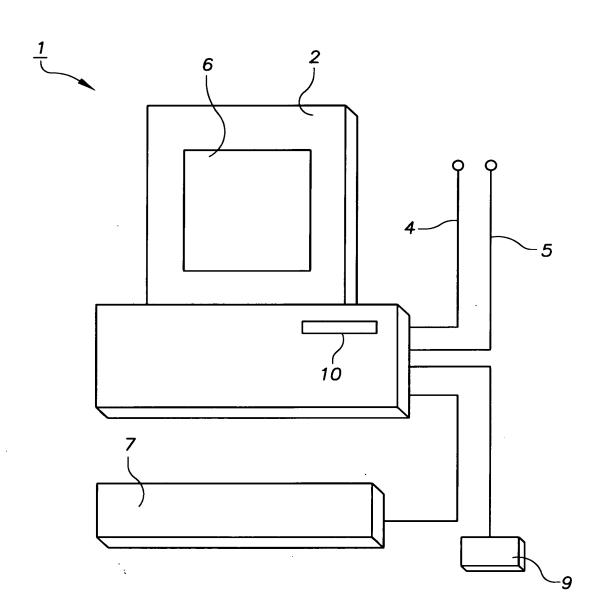
FIG. 1



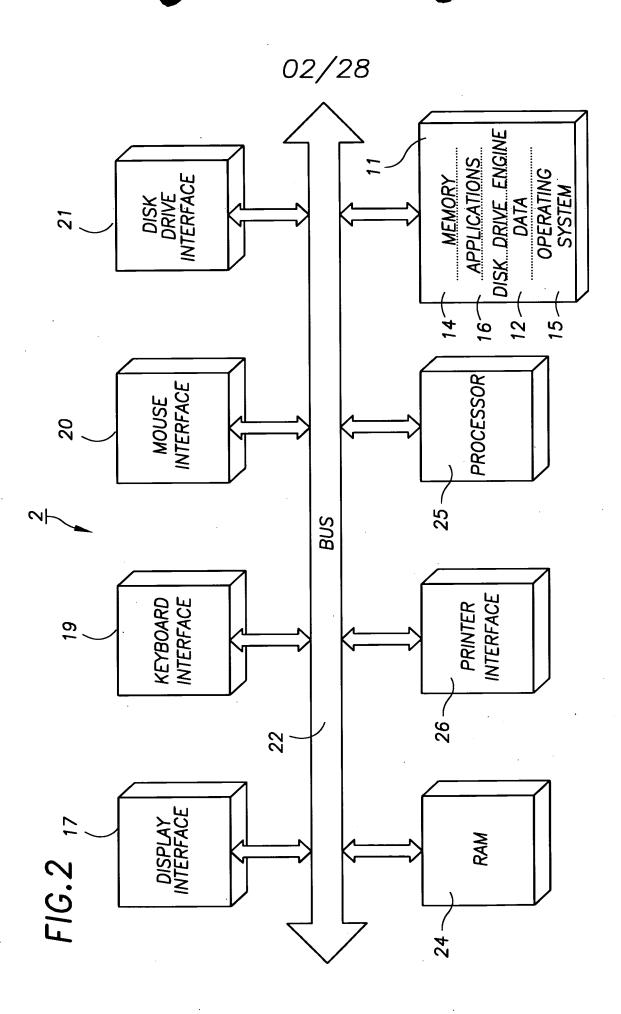
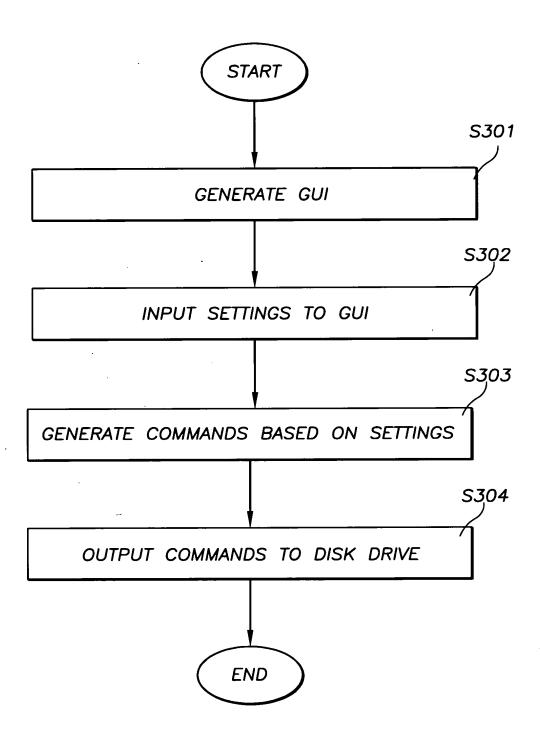


FIG.3



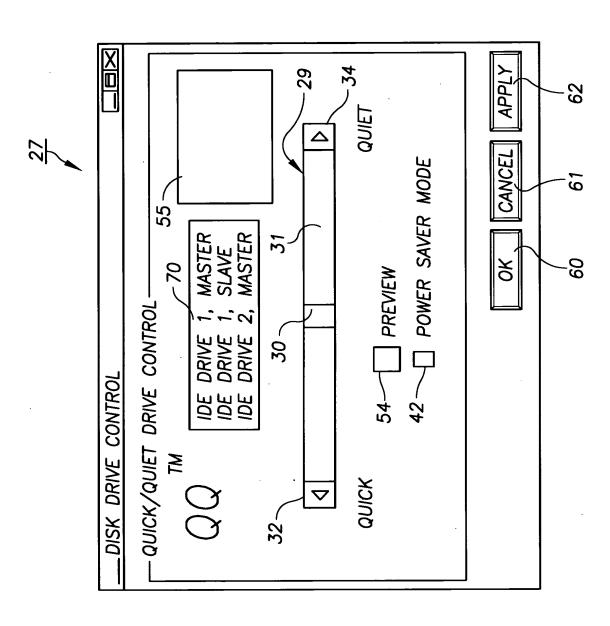
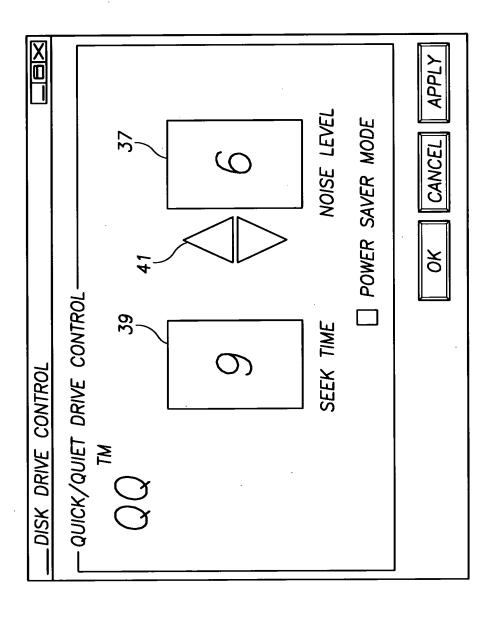
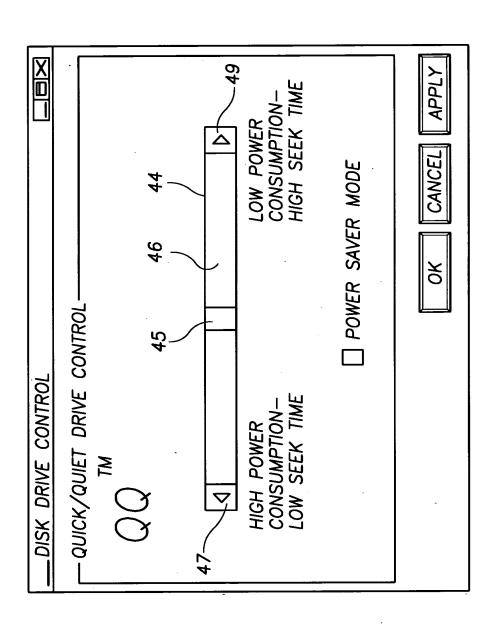


FIG.4



F1G.5



F1G.6

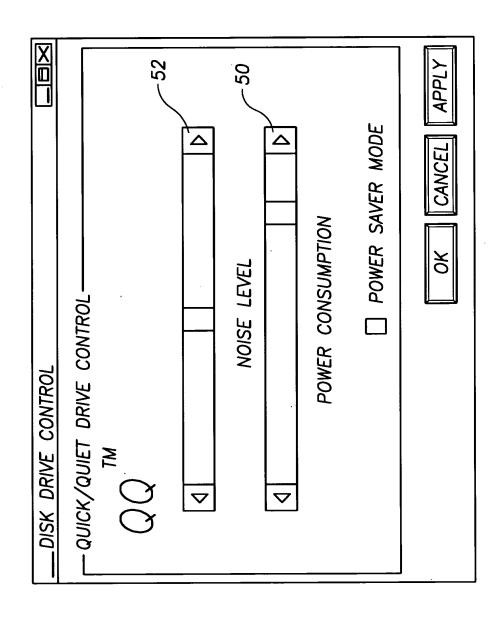
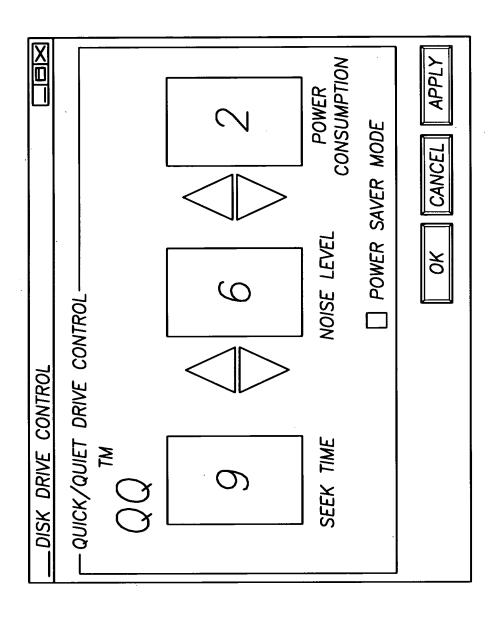


FIG.7



F1G.8

IDE DRIVE 1, MASTER

IDE DRIVE 1, SLAVE

IDE DRIVE 2, MASTER

F1G.9

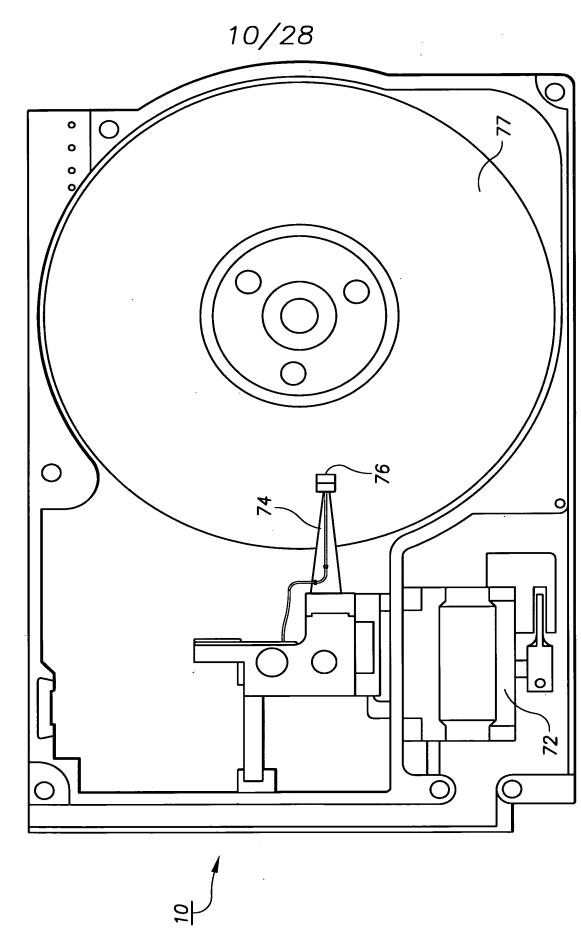
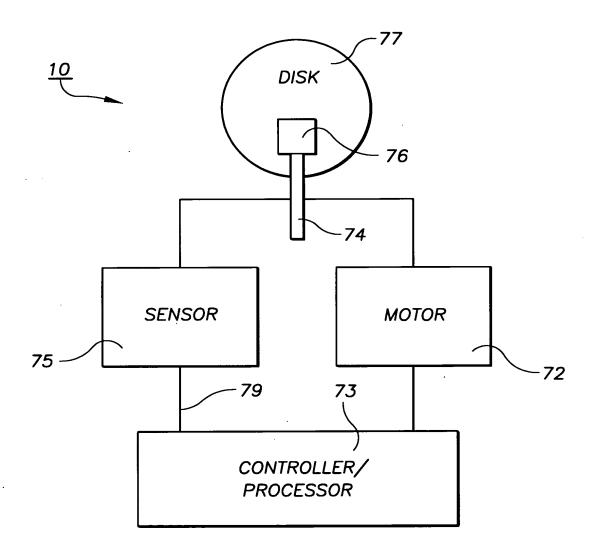


FIG. 10A

FIG. 10B



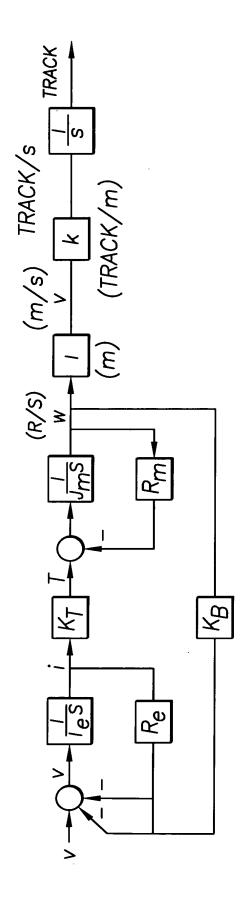
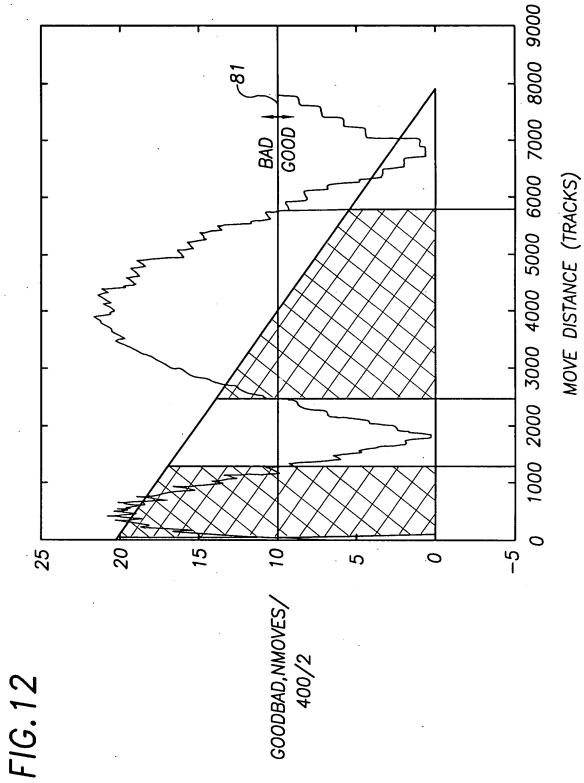


FIG. 11



14/28

FIG. 13
PRIOR ART

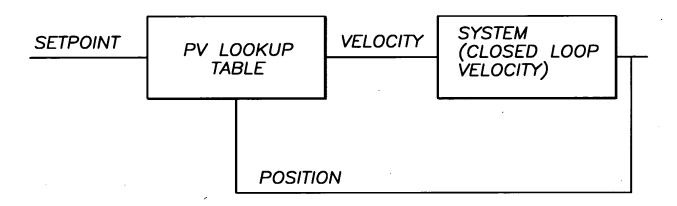


FIG. 14

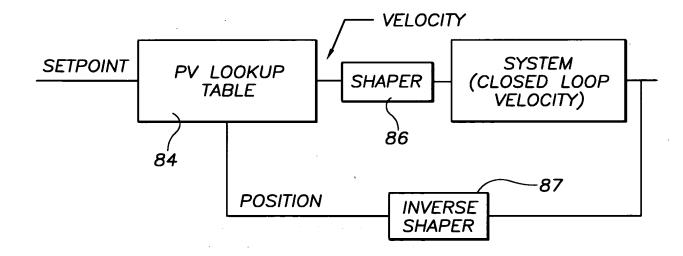


FIG. 15

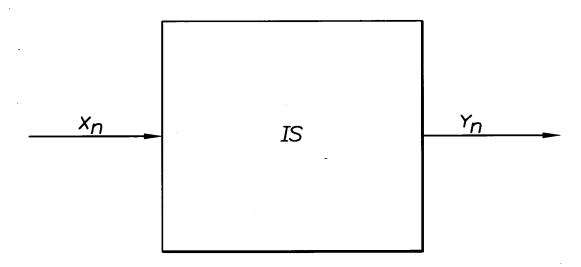


FIG. 16

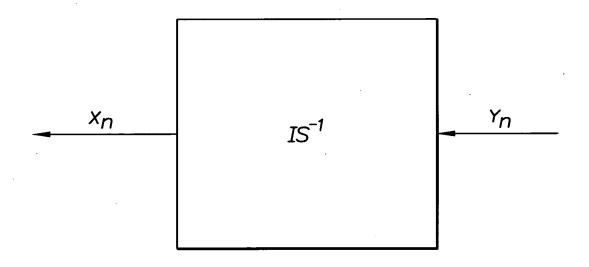


FIG. 17

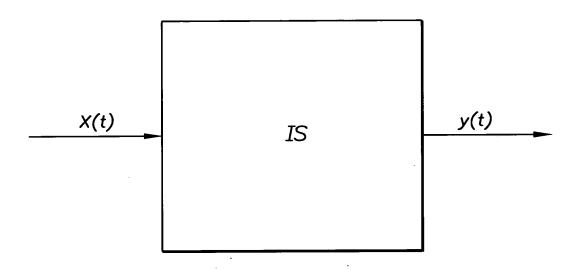


FIG18

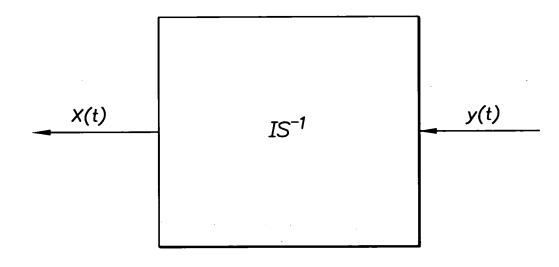


FIG. 19

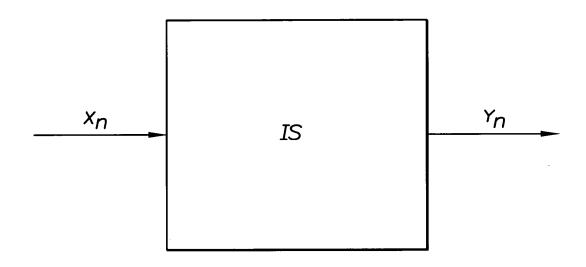
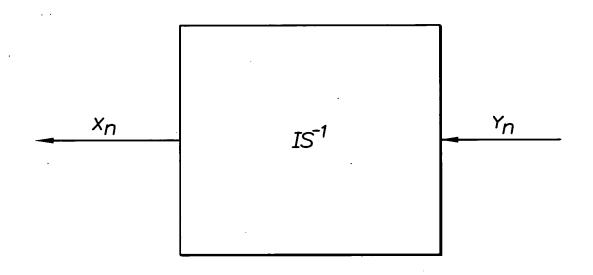


FIG20



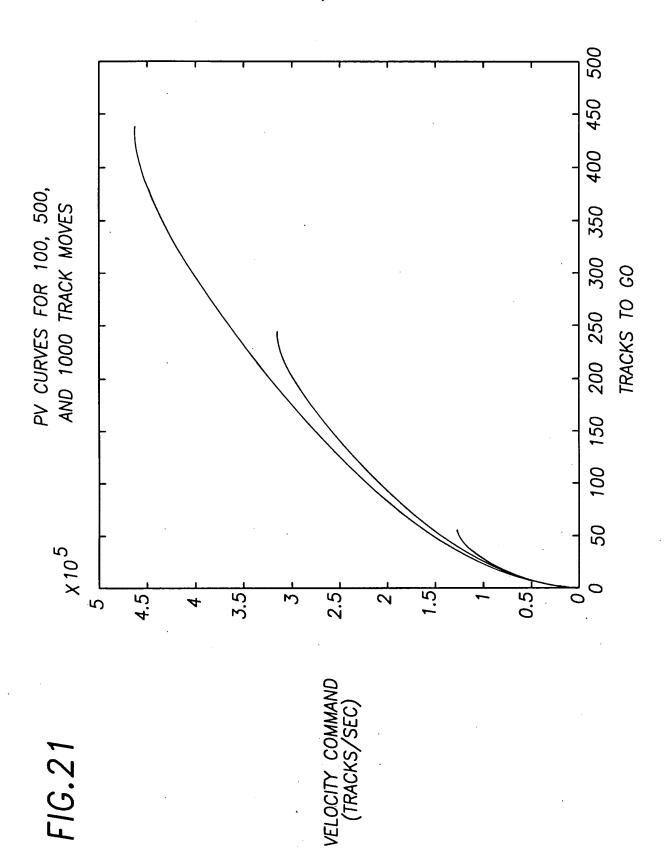
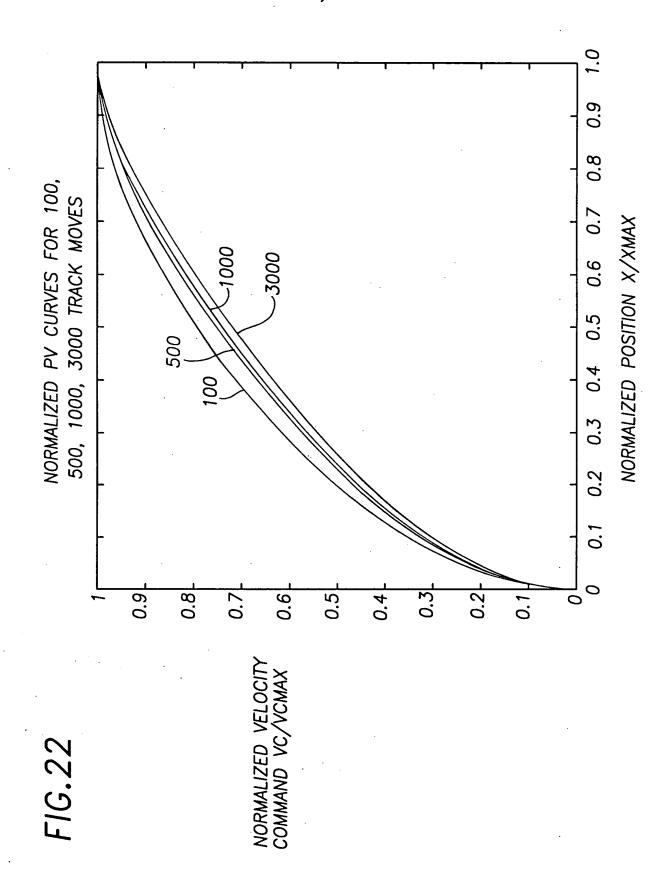
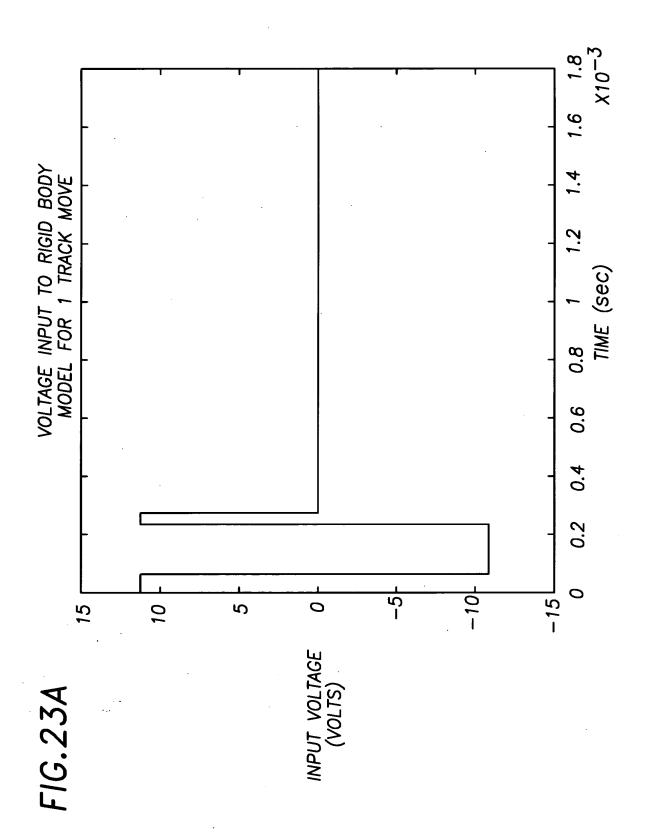
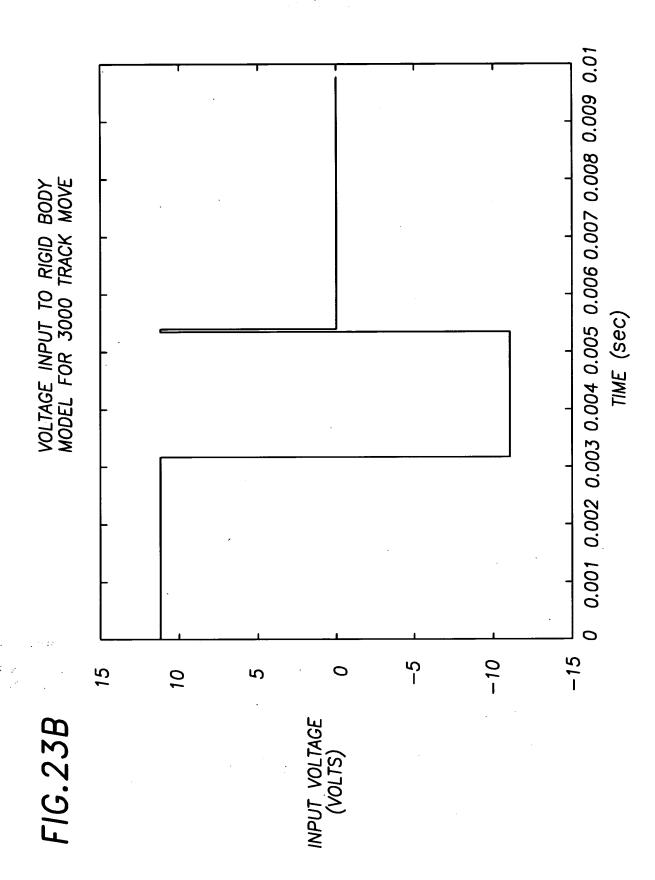


FIG.21







22/28

FIG.24

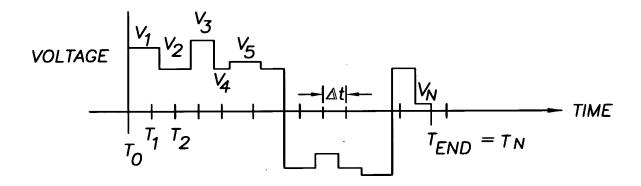


FIG.25

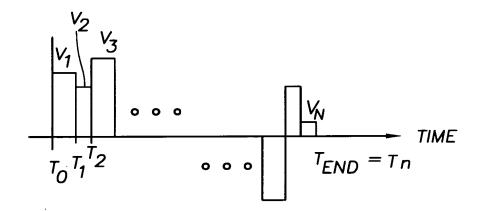


FIG.26

$$\begin{array}{c|c} V_1 & V_2 & V_N \\ \hline \hline T_1 & T_2 & + & 0 & 0 & + & T_{END} \\ \hline \hline T_0 & -V_1 & -V_2 & -V_N & -V_N \\ \hline \end{array}$$

FIG.27

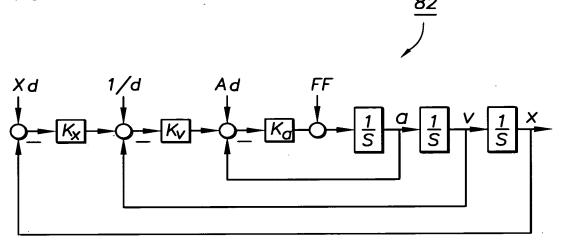
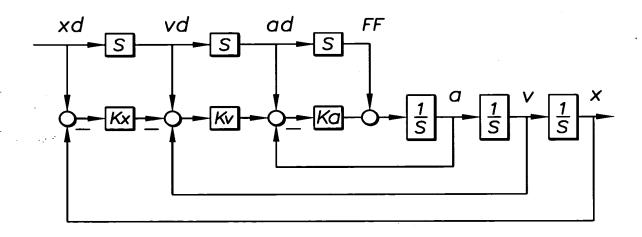
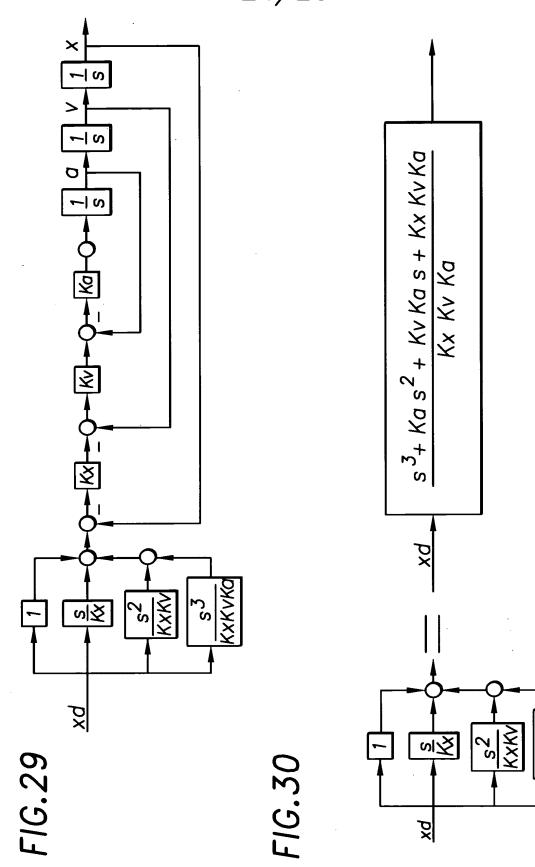


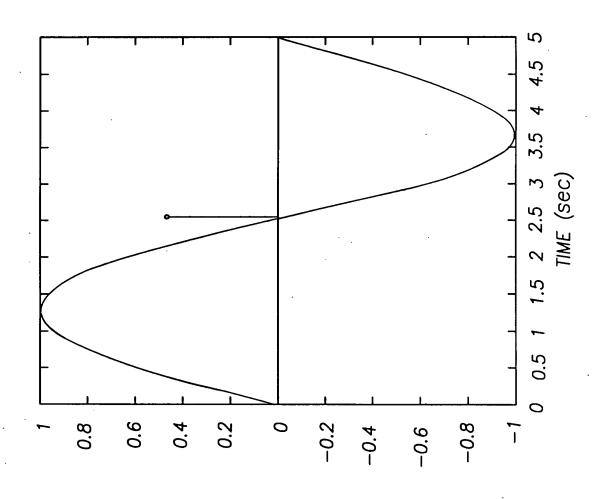
FIG.28





s3 KXKVKa

F1G.31



AMPLITUDE

FIG.32

FIG.33

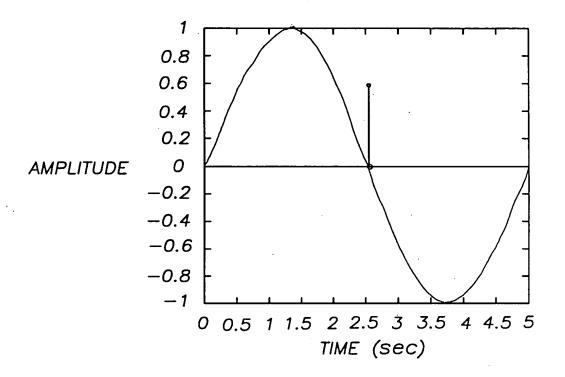


FIG. 34

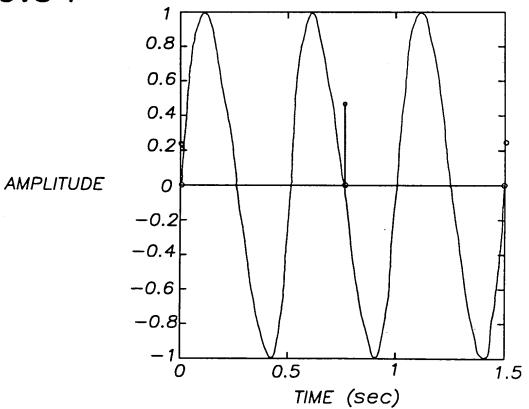


FIG.35

